

ISSUE CLASSIFICATION	
Class	Subclass

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<p>O.I.P.E.</p> <p>SCANNED <i>HK 30.A. Dec 3</i></p>	<p>PATENT DATE</p>
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APPLICATION NO. 09/807500	CONT/PRIOR D	CLASS 2	SUBCLASS 2	ART UNIT 2 2709	EXAMINER Do
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APPLICANTS

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TITLE

Area efficient, realization of coefficient architecture for bit-serial fir, iir filters and combinational/sequential logic structure with zero latency clock output

PTO-2040
12/89

ISSUING CLASSIFICATION															
ORIGINAL				CROSS REFERENCE(S)											
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
INTERNATIONAL CLASSIFICATION															

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		NOTICE OF ALLOWANCE MAILED	
	_____ (Primary Examiner) (Date)		ISSUE FEE	
Amount Due			Date Paid	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____				
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